IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaowei Deng, et al.	Docket No:	TI-31071
Serial No:	09/976,983	Conf. No:	3329
Examiner:	Trong Q. Phan	Art Unit:	2818
Filed:	10/12/2001		
For:	LOADLESS 4T SRAM CELL WITH PMOS DRIVERS		

APPEAL BRIEF UNDER 37 C.F.R. 1.192

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this Appeal Brief filed, in triplicate, under 37 CFR 1.192 is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, DC 20231 on 10-30-02.

Ann Trent
Ann Trent

Assistant Commissioner of Patents
Washington, D. C. 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final rejection mailed June 7, 2002, and the Advisory Action mailed August 27, 2002.

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Real Party in Interest under 37 C.F.R. 1.192(c)(1)

Texas Instruments Incorporated is the real party in interest.

Related Appeals and Interferences under 37 C.F.R. 1.192 (c)(2)

There are no related appeals or interferences known to appellant, the appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the board's decision in the pending appeal.

Status of Claims on Appeal under 37 C.F.R. 1.192 (c)(3)

Claims 1 and 2 are pending in this case. Claims 1 and 2 are appealed.

Status of Amendments Filed After Final rejection under 37 C.F.R. 1.192 (c)(4)

An amendment pursuant to 37 CFR 1.116 was filed on 8-12-2002. The examiner did not enter the amendment.

Summary of the Invention under 37 C.F.R. 1.192(c)(5)

The instant invention is a memory cell that operates over a wide range of temperatures. The memory cell has numerous advantages over memory cell structures used in the art.

The memory cell of the instant invention is formed by interconnecting PMOS drive transistors and NMOS pass transistors to wordlines, bitlines, and a supply voltage. In particular a PMOS drive transistor has one of its source/drain terminals connected to a supply voltage. The other source/drain terminal of the PMOS drive transistor is connected to a first storage node and the gate terminal of the PMOS drive transistor is connected to second storage node (page 5, lines 7-21). A NMOS pass transistor has one of its source/drain terminals connected to a bitline. The second source/drain terminal of the NMOS pass transistor is connected to the first storage node and the gate terminal of the NMOS pass transistor is connected to a wordline (page 5, lines 21-30).

An important condition of the memory cell is that for the same voltages applied across the gate and source/drain terminals of the NMOS pass transistor and the gate and source/drain terminals of the PMOS drive transistor, the current which flows through the source/drain terminal of the NMOS pass transistor must be greater than the current which flows through the source/drain terminal of the PMOS drive transistor. The condition applies to all NMOS and PMOS transistors in the memory cell. This condition can be achieved using well-known NMOS and PMOS transistor design and processing techniques (page 5, lines 32-33, page 6, lines 1-10).

Statement of Issues Presented for Review under 37 C.F.R. 1.192 (C)(6)

1. Are claims 1 and 2 properly rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most connected, to make and/or use the invention?

2. Are claims 1 and 2 properly rejected under 35 U.S.C. 102(a) as being anticipated by Portacci (6,172,901)?

Statement of the Grouping of Claims under 37 C.F.R. 1.192(C)(7)

Claims 1 and 2 stand or fall together.

Arguments

1. Are claims 1 and 2 properly rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most connected, to make and/or use the invention?

Patent owner respectfully submits that claims 1 and 2 are not properly rejected under 35 U.S.C. 112.

The specification states that for the same voltages applied to the terminals of the NMOS pass transistor and the PMOS drive transistor the current flowing through the NMOS transistor must be greater than the current flowing through the PMOS transistor (page 5, lines 32-33 and page 6, lines 1-10). This is described in the specification as "a condition" of the memory cell. In forming the rejection under 35 U.S.C. 112 the examiner ignores the clear meaning of the condition and argues instead that the described condition occurs during circuit operation. The operation of the circuit is described starting on page 6, line 11, which states "[I]n operation .....". Rather than describing circuit

operation the above-described condition simply describes what transistor current values should result if the same voltages are applied to a NMOS transistor and a PMOS transistor used to form the memory cell. The current that results when voltages are applied to the terminals of a NMOS or PMOS transistor is a function of the design and processing conditions of the transistor. Factors such as threshold voltage, gate length, and gate dielectric layer thickness can all affect the resulting current. This idea is expressed in the specification on page 6, lines 9 and 10. There it states, "[T]his condition can be achieved using well known NMOS and PMOS transistor design and processing techniques." The statement further highlights the idea that the condition for resulting transistor current refers to the NMOS and PMOS transistors individually and not to the memory cell circuit operation as suggested by the examiner.

The examiner states that there is no antecedent basis for "the same voltages" on line 21 of claim 1. Referring to page 5, lines 32-33, it is stated in the disclosure that for the same voltages applied across the gate and source/drain terminals of the NMOS and PMOS transistors the resulting current in the NMOS transistor must be greater than the current in the PMOS transistor. There is clearly antecedent basis for "the same voltages" in claim 1.

2. Are claims 1 and 2 properly rejected under 35 U.S.C. 102(a) as being anticipated by Portacci (6,172,901)?

Applicant respectfully submits that caims 1 and 2 are not properly rejected under 35 U.S.C. 102(a) as being anticipated by Portacci.

In the Portacci patent (6,172,901) column 7, lines 23-30 states, "When using PMOS transistors for the pass transistors 226, 236, the designer must be aware that the reading current will be less than if NMOS transistors are used, such as in the memory cell 110." This is a statement comparing PMOS and NMOS transistors for use as pass transistors. The Portacci patent therefore does not describe that the current flowing through each of the PMOS drive transistors is less than the current flowing through the

NMOS transistor as required claim 1 and 2 of the instant invention. Claims 1 and 2 are therefore not properly rejected under 35 U.S.C. 102(a) as being anticipated by Portacci.

Conclusion

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1 and 2 under 35 U.S.C. § 102(a) and under 35 U.S.C. 112(1) is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants' petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

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APPENDIX

Claims on Appeal

1. A memory cell, comprising:

providing a PMOS drive transistor with a gate terminal, a first source/drain terminal, and a second source/drain terminal;

providing a NMOS pass transistor with a gate terminal, a first source/drain terminal and a second source/drain terminal;

connecting said first source/drain terminal of said NMOS pass transistor to a bitline;

connecting said second source/drain terminal of said NMOS pass transistor to a first storage node;

connecting said gate terminal of said NMOS pass transistor to a wordline;

connecting said first source/drain terminal of said PMOS drive transistor to a supply voltage;

connecting said second source/drain terminal of said PMOS drive transistor to said first storage node;

connecting said gate terminal of said PMOS drive transistor to a second storage node; and

wherein a current flowing through the source/drain terminals of the NMOS pass transistor is greater than a current flowing through the source/drain terminals of the PMOS drive transistor for the same voltages applied between the gate and source/drain

terminals of the PMOS drive transistor and the gate and source/drain terminals of the NMOS pass transistor.

2. The memory cell of claim 1 wherein during a read operation a voltage applied to the wordline is less than 90% of the supply voltage.